

Ultra-Low-Latency SmartNIC for Deterministic Trading

Napatech NT200A02-03-ULL SmartNIC

A Complete ULL Trading Platform



Ethernet



Network Acceleration



PCIe Connectivity

ULL Ethernet MAC/PCS

ULL TCP/IP UDP/IP Offload Engine

ULL PCIe DMA Controller

EXECUTE ON INFORMATION, NOT PACKETS.

Financial performance in electronic trading heavily relies on ultra-low latency (ULL), deterministic execution, and nanosecond wire-to-wire processing. The Napatech NT200A02-03-ULL Trading Platform turns raw market feeds into actionable execution intelligence by offloading complete L2-L4 network processing into dedicated FPGA soft logic. By handling session state, protocol decoding, and line-rate transactions on-chip, infrastructure teams eliminate operating system jitter, bypass kernel overhead, and achieve predictable tick-to-trade latency under extreme market volatility.

WHAT IT DELIVERS



Ultra-Low-Latency Tick-to-Trade Platform
Offload L4 TCP/UDP state tracking directly to user FPGA logic with nanosecond processing latency in hardware cut-through mode.



Real-Time Market Data Feed Handler
FPGA offload of parsing, decoding, and normalization of market data, providing ultra-low-latency throughput.



Smart Order Routing
Real-time FPGA logic to evaluate venues and route orders with a hardware-level decision process.



Real-Time Pre-Trade Risk Checks
Hardware-accelerated validation engines to perform risk checks.



Real-Time Visibility and Monitoring
Hardware timestamps and microburst detection.



Preserve Determinism Under Load
Maintain continuous line-rate performance with zero dropped frames.



Multiple High-Speed Ports
Two QSFP28 ports with 100 or 25G connections (see product data sheet for details).

Napatech NT200A02-03-ULL

AMD/Xilinx VU5P-3 FPGA

1 Ethernet MAC/PCS TCP/IP Offload Engine

2 Ethernet MAC/PCS TCP/IP Offload Engine

3 Ethernet MAC/PCS UDP/IP Offload Engine

FPGA Application (Business Logic)

PCle Circular Buffer DMA (CDMA) Controller

PCle High-Performance Computing Server

CPU Host Memory

Software Framework (Kernel & User space)

Software Application (User space)

Napatech ULL IP

User Programmable

FPGA Full Loopback RIT Latency

- 1 • MAC/PCS: 20.1ns⁽¹⁾ - TxSoPacket to RxSoFrame
- 2 • MAC/PCS + TCP/IP: 90.0ns⁽¹⁾ - TxSoPacket to RxSoPayload
- 3 • MAC/PCS + UDP/IP: 80.7ns⁽¹⁾ - TxSoPacket to RxSoPayload

FPGA - Host Loopback RTT Latency

- 4 • ULL PCIe CDMA RTT Latency

Payload Size (B)	RTT Latency (ns)
0	~580
100	~600
200	~650
300	~700
400	~720
500	~750

Test Conditions / Notes

- PCIe gen 3 x 8
- Host: Intel(R) Core(TM) i7-9700 CPU (Base: 3.00GHz, Turbo: 4.70GHz)
- Minimum latency (128k packets are sent out for each payload size)
- Linux OS: CentOS 7
- FPGA: VU5P (-2 speed grade)
- ⁽¹⁾ Expected latencies when operating with VU5P-3 speed grade FPGA (644MHz)

Accelerate Your Trading. Differentiate Your Solution.
Napatech provides the accelerated trading platform.
You own the trading application and your implementation of the IP.

napatech.com

Napatech NT200A02-03-ULL TradingPlatform

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